This listing of claims replaces all prior listings of the claims in the application.

In the Claims:

1. (canceled)

2. (previously presented) The method of Claim 25 wherein said integrated circuit memory is of the type selected from dynamic random access memory DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.

3. (previously presented) The method of Claim 25 wherein said failed memory element is replaced with a redundancy element selected from the group consisting of at least row redundancy element and column redundancy element.

4-11. (canceled)

12. (currently amended) The method of Claim ~~11~~ 25 wherein said ~~failed memory element is automatically replaced~~ fusible elements are electrically activated when said integrated circuit remains installed within a product for normal use.

13. (canceled)

14. (previously presented) The integrated circuit of Claim 26 wherein said memory is of the type selected from dynamic random access memory (DRAM), static random access memory (SRAM), and electrically erasable programmable read only memory (EEPROM) including flash memory.

15-16. (canceled)

17. (currently amended) The integrated circuit of Claim 26 wherein said means for automatically identifying a failed memory element identifies said failed memory

element while said integrated circuit is in a normal operational mode and said means for electrically activating said fusible elements activates said fusible elements ~~said failed memory element is identified and replaced~~ while said integrated circuit is in a normal operational mode.

18-20. (canceled)

21. (previously presented) The integrated circuit of Claim 26 wherein said integrated circuit includes a microprocessor.

22. (currently amended) The integrated circuit of Claim ~~20~~ 26 wherein said memory is of the DRAM type and wherein said means for recording records said locations of said failures ~~are recorded~~ while said integrated circuit is in a normal operational mode.

23. (canceled)

24. (previously presented) The integrated circuit of Claim 26 wherein said redundancy element is selected from the group consisting of at least row redundancy element and column redundancy element.

25. (currently amended) A method for identifying a failed memory element within an integrated circuit memory and for repairing said integrated circuit memory, comprising:

providing an integrated circuit memory having a plurality of banks;

automatically identifying and recording locations of failures within said integrated circuit memory by storing data bits and error correction code ("ECC") check bits to individual locations of said integrated circuit memory;

thereafter retrieving data bits and ECC check bits from said individual locations;

recording at least single-bit failure locations in said integrated circuit memory based on ECC processing said retrieved data bits together with said retrieved ECC check bits;

based on said recorded failure locations, using first logic circuits within said integrated circuit to automatically identify a failed memory element in one bank of said plurality of banks; and

asserting a busy signal for said one bank ~~while servicing memory access requests by banks of said plurality of banks other than said one bank~~; and

while asserting said busy signal and servicing at least one of read or write access requests to banks of said plurality of banks other than said one bank, electrically activating fusible elements ~~using at least second logic circuits~~ within said integrated circuit including elements selected from the group consisting of fuses and antifuses, to electrically alter circuit connections of said integrated circuit memory to automatically replace said failed memory element in said one bank with a redundancy element.

26. (currently amended) An integrated circuit including a self-repairing memory having a plurality of banks, comprising:

a memory;

error correction code (ECC) logic circuits coupled to said memory, said ECC logic circuits operable to detect errors within strings of data bits and check bits retrieved from addressed storage locations within said memory;

means for recording locations of at least single-bit failures from said detected errors;

means for automatically identifying a failed memory element in one of said

plurality of banks based on said recorded locations;

means for asserting a busy signal for said one bank;

electrically activatable fusible elements including elements selected from the group consisting of fuses and antifuses; and

means for electrically activating at least some of said fusible elements to electrically alter circuit connections of said memory to automatically ~~replacing~~ replace said failed memory element in said one bank with a redundancy element~~; and~~

~~means for providing~~ while said busy signal is asserted; and

means for permitting at least one of read access or write access to banks of said plurality of banks other than said one bank while said busy signal is asserted ~~while said failed memory element is identified and replaced~~.

27. (canceled)